UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,012	12/31/2003	Suresh Rajgopal	03-LJ-017	9337

30425 7590 06/23/2011

STMICROELECTRONICS, INC.
MAIL STATION 2346
750 CANYON DRIVE, SUITE 300
COPPELL, TX 75019

EXAMINER	
ZHU, BO HUI ALVIN	

ART UNIT	PAPER NUMBER
2465	

NOTIFICATION DATE	DELIVERY MODE
06/23/2011	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

angie.rodriguez@st.com
ip.us@st.com

Office Action Summary	Application No.	Applicant(s)	
	10/750,012	RAJGOPAL ET AL.	
	Examiner	Art Unit	
	BO HUI A. ZHU	2465	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 February 2011*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 3, 5—14, 16 and 18 - 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hariguchi et al. (US 6,665,297) in view of Douceur (US 6,067,547), and further in view of Frank et al. (US 7,194,740).

(1) Regarding claims 1 and 14:

Hariguchi et al. discloses a system and method, comprising: a plurality of hash tables (82-8 -- 82-32, Fig. 2A) each storing prefixes for address lookups; and a content addressable memory (80, Fig. 2A) storing at least some prefixes for which a collision occurs within at least one of the hash tables (column 6, lines 31 – 39); and a hashing lookup search mechanism that comprises a routing table (40, Fig. 2A) implemented with selective hashing for a plurality of prefixes with different lengths (column 5, lines 20 – 24); and a plurality of memory blocks (memory for each hash bucket 160), wherein each hash table is allocated a group of the memory blocks. (column 6, line 66 – column 7, line 2; column 8, line 56 - column 9, lines 7; each hash circuit comprises a hash bucket which comprises certain amount of memory for storing route entries, see 160, Fig. 4); and a configuration register (mask circuit, 154, Fig. 4) associated with reach memory

block, each configuration register identifying the prefix length to which the respective memory block is allocated (e.g. see column 6, lines 54 – 61).

Hariguchi et al. does not disclose each hash table is allocated a group of the memory blocks based on a size of the respective hash table and a pre-assigned maximum number of allocated blocks.

Douceur teaches a hash table is allocated a group of memory blocks based on a size of the respective hash table (column 19, line 23 – 26; line 62 - 67).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of Hariguchi to include the features of allocating a group of the memory blocks to each hash table based on a size of the respective hash table, as suggest by Douceur for the purpose of more efficient usage of memory resource.

Frank et al. teaches allocating memory based on a pre-assigned maximum number of memory (column 5, line 31 – 34).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of Hariguchi to include the feature of allocating memory based on a pre-assigned maximum number of memory as shown in Frank et al. for the purpose of improving efficiency by limiting the memory blocks each hash table can be assigned.

(2) Regarding claims 3 and 16:

Hariguchi et al. in view of Douceur and Frank et al. discloses all of the subject matter as discussed in the rejection of claims 1 and 14.

Hariguchi et al. does not disclose each hash table is allocated no more than a predefined number of memory blocks.

Frank et al. teaches allocating memory no more than the pre-assigned maximum number of memory blocks (column 5, line 31 – 34).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of Hariguchi to include the feature of each hash table is allocated no more than a predefined number of memory blocks as shown in Frank et al. for the purpose of improving efficiency by limiting the memory blocks each hash table can be assigned.

(3) Regarding claims 5 and 18:

Hariguchi et al. further discloses each hash table containing different length prefixes (column 5, lines 20 – 31, hash table 70 comprises a plurality of hash circuit 82; each hash circuit 82 determines a match based on a predetermined portion of the address using its associated prefix length).

(4) Regarding claims 6 and 19:

Hariguchi et al. further discloses a priority encoder (172, Fig. 5) selecting a longest prefix when a plurality of matches occur between different length portions of a prefix and prefixes in each of two or more of the plurality of hash tables (column 8, lines 4 – 8)

(5) Regarding claims 7 and 20:

Hariguchi et al. further discloses that the plurality of hash tables contain only a subset of different length prefixes possible under an addressing scheme, and wherein a

remainder of the different length prefixes are stored in the content addressable memory (column 6, lines 30 – 39).

(6) Regarding claim 8:

Hariguchi et al. discloses a system comprising: an address lookup structure that includes: a plurality of hash tables (82-8 -- 82-32, Fig. 2A) each storing prefixes for address lookups; and a content addressable memory (80, Fig. 2A) storing at least some prefixes for which a collision occurs within at least one of the hash tables (column 6, lines 31 – 39); and a hashing lookup search mechanism that comprises a routing table (40, Fig. 2A) implemented with selective hashing for a plurality of prefixes with different lengths (column 5, lines 20 – 24); and a plurality of memory blocks (memory for each hash bucket 160), wherein each hash table is allocated a group of the memory blocks. (column 6, line 66 – column 7, line 2; column 8, line 56 - column 9, lines 7; each hash circuit comprises a hash bucket which comprises certain amount of memory for storing route entries, see 160, Fig. 4); and a configuration register (mask circuit, 154, Fig. 4) associated with reach memory block, each configuration register identifying the prefix length to which the respective memory block is allocated (e.g. see column 6, lines 54 – 61); a network search engine (70, Fig. 2A) containing the at least one hash table and coupled to the content addressable memory, the network search engine performing address lookups using the at least one hash table; and an external memory (98, Fig. 2A) coupled to the network search engine and containing per route information indexed by a next hop index generated by the network search engine

Hariguchi et al. does not disclose each hash table is allocated a group of the memory blocks based on a size of the respective hash table and a pre-assigned maximum number of allocated blocks.

Douceur teaches a hash table is allocated a group of memory blocks based on a size of the respective hash table (column 19, line 23 – 26; line 62 - 67).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of Hariguchi to include the features of allocating a group of the memory blocks to each hash table based on a size of the respective hash table, as suggest by Douceur for the purpose of more efficient usage of memory resource.

Frank et al. teaches allocating memory based on a pre-assigned maximum number of memory (column 5, line 31 – 34).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of Hariguchi to include the feature of allocating memory based on a pre-assigned maximum number of memory as shown in Frank et al. for the purpose of improving efficiency by limiting the memory blocks each hash table can be assigned.

(7) Regarding claim 9:

Hariguchi et al. discloses a network (20, Fig. 1) including a plurality of interconnected network routers (26, 28, 30 – 38, Fig. 1), wherein at least one of the plurality of network routers comprises: an address lookup structure that includes: a plurality of hash tables (82-8 -- 82-32, Fig. 2A) each storing prefixes for address lookups; and a content addressable memory (80, Fig. 2A) storing at least some prefixes

for which a collision occurs within at least one of the hash tables (column 6, lines 31 – 39); and a hashing lookup search mechanism that comprises a routing table (40, Fig. 2A) implemented with selective hashing for a plurality of prefixes with different lengths (column 5, lines 20 – 24); and a plurality of memory blocks (memory for each hash bucket 160), wherein each hash table is allocated a group of the memory blocks. (column 6, line 66 – column 7, line 2; column 8, line 56 - column 9, lines 7; each hash circuit comprises a hash bucket which comprises certain amount of memory for storing route entries, see 160, Fig. 4); and a configuration register (mask circuit, 154, Fig. 4) associated with reach memory block, each configuration register identifying the prefix length to which the respective memory block is allocated (e.g. see column 6, lines 54 – 61); a network search engine (70, Fig. 2A) containing the at least one hash table and coupled to the content addressable memory, the network search engine performing address lookups using the at least one hash table; and an external memory (98, Fig. 2A) coupled to the network search engine and containing per route information indexed by a next hop index generated by the network search engine

Hariguchi et al. does not disclose each hash table is allocated a group of the memory blocks based on a size of the respective hash table and a pre-assigned maximum number of allocated blocks.

Douceur teaches a hash table is allocated a group of memory blocks based on a size of the respective hash table (column 19, line 23 – 26; line 62 - 67).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of Hariguchi to include the features of allocating a group

of the memory blocks to each hash table based on a size of the respective hash table, as suggest by Douceur for the purpose of more efficient usage of memory resource.

Frank et al. teaches allocating memory based on a pre-assigned maximum number of memory (column 5, line 31 – 34).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of Hariguchi to include the feature of allocating memory based on a pre-assigned maximum number of memory as shown in Frank et al. for the purpose of improving efficiency by limiting the memory blocks each hash table can be assigned.

(8) Regarding claim 10:

Hariguchi et al. discloses that a plurality of hash tables, each hash table containing different length prefixes (column 5, lines 20 – 31); each hash table containing different length than prefixes within other hash tables with in the plurality (column 5, lines 20 – 31); and the plurality of hash tables collectively containing only a subset of different prefix lengths less than or equal to an address lengths and a remainder of the different address lengths are handled by an additional address lookup facility (column 6, lines 30 – 39); and a hashing search mechanism that comprises a routing table (40, Fig. 2A) implemented with selective hashing for a plurality of prefixes with different lengths (column 5, lines 20 – 24); and a plurality of memory blocks, wherein each hash table is allocated a group of the memory blocks. (column 6, line 66 – column 7, line 2; column 8, line 56 - column 9, lines 7; each hash circuit comprises a hash bucket which comprises memory blocks for storing route entries, see 160, Fig. 4; memory blocks are inherent

because each hash bucket stores route entries such as network addresses); and a configuration register (mask circuit, 154, Fig. 4) associated with reach memory block, each configuration register identifying the prefix length to which the respective memory block is allocated (e.g. see column 6, lines 54 – 61).

Hariguchi et al. does not disclose each hash table is allocated a group of the memory blocks based on a size of the respective hash table and a pre-assigned maximum number of allocated blocks.

Douceur teaches a hash table is allocated a group of memory blocks based on a size of the respective hash table (column 19, line 23 – 26; line 62 - 67).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of Hariguchi to allocate a group of the memory blocks to each hash table based on a size of the respective hash table as suggest by Douceur in order to make use of memory resource more efficient.

Frank et al. teaches allocating memory based on a pre-assigned maximum number of memory (column 5, line 31 – 34).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of Hariguchi to include the feature of allocating memory based on a pre-assigned maximum number of memory as shown in Frank et al. for the purpose of improving efficiency by limiting the memory blocks each hash table can be assigned.

(9) Regarding claim 11:

Hariguchi et al. further discloses the additional address lookup facility comprises a content addressable memory (80, Fig. 2A; column 6, lines 30 – 39).

(10) Regarding claim 12:

Hariguchi et al. further discloses each of the plurality of hash tables in contained in one or more memory blocks allocated based on hashing of each prefix contained in the respective hash table using at least a first hash function (inherent be cause hash tables inherently use hash functions), and wherein a remainder of prefixes of a length corresponding to prefixes within the respective hash table are handled by the additional address lookup facility (column 6, lines 30 – 39).

Hariguchi et al. does not disclose a number of memory blocks allocated to the respective hash table does not exceed a predefined number.

Frank et al. teaches allocating memory no more than the pre-assigned maximum number of memory blocks (column 5, line 31 – 34).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of Hariguchi to include the feature of a number of memory blocks allocated to the respective hash table does not exceed a predefined number as shown in Frank et al. for the purpose of improving efficiency by limiting the memory blocks each hash table can be assigned.

(11) Regarding claim 13:

Hariguchi et al. further discloses a priority encoder (172, Fig. 5) selecting a longest prefix match from matches identified within the plurality of hash tables (column 8, lines 4 – 8).

(12) Regarding claim 21:

Hariguchi et al. further discloses the configuration register identifies a prefix length between sixteen (16) and thirty-two (32) bits (column 6, line 56 – 61).

(13) Regarding claim 22:

Hariguchi et al. further discloses a configuration register (mask circuit, 154, Fig. 4) identifies the hash function to which the respective memory block is allocated (e.g. see column 6, lines 54 – 61).

3. Claims 2 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hariguchi et al. (US 6,665,297) in view of Douceur (US 6,067,547) and Frank et al. (US 7,194,740), and further in view of McMahon et al. (US 5,784,699).

(1) Regarding claims 2 and 15:

Hariguchi et al. in view of Douceur and Frank et al. discloses all of the subject matter as discussed in the rejection of claims 1 and 14. Hariguchi et al. further discloses each hash table holds prefixes for which no collision occurs within the hash table (column 6, lines 31 – 39; column 9, lines 12 – 15).

Hariguchi et al. does not disclose each hash table is allocated a smallest number of memory blocks sufficient to hold entries within the hash table.

McMahon et al. teaches allocating a smallest number of memory blocks sufficient for use (column 3, line 54 – 58).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of Hariguchi to allocate a smallest number of memory

blocks sufficient to each hash table as suggest by McMahon et al. in order to make use of memory more efficient.

4. Claims 4 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hariguchi et al. (US 6,665,297) in view of Delaney et al. (US 2001/0027479) and Frank et al. (US 7,194,740), and further in view of Tal et al. (US 6,625,612).

(1) Regarding claims 4 and 17:

Hariguchi et al. in view of Douceur and Frank et al. discloses all of the subject matter as discussed in the rejection of claims 1 and 14. Hariguchi et al. further discloses the at least one hash table (70, Fig. 2A) contains prefixes hashed by one hash functions.

Haiguchi et al. does not disclose a second of the two hash functions employed when a collision occurs with a first of the two hash functions.

Tal et al. teaches using two hash functions and a second of the two hash functions employed when a collision occurs with a first of the two hash functions (column 1, lines 54 – 59).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of Hariguchi et al. to include the features of a second of the two hash functions employed when a collision occurs with a first of the two hash functions, as shown in Tal et al. for the purpose of more efficiently resolving hash collisions.

Response to Arguments

5. Applicant's arguments filed on 02/07/2011 with respect to claim 1 have been considered but are not persuasive. Specifically, applicant argues that Frank does not teach memory blocks are allocated based on a pre-assigned maximum number of allocated blocks (PRE-APPEAL BRIEF, page 3). Examiner respectfully disagrees. Frank teaches a memory allocation process in which the requested memory is compared to a maximum value supported by the operating system, and memory is allocated based on the result of the comparison (column 5, lines 26 - 43). Applicant contends that the maximum limit imposed by the operating system for requested memory is not "pre-assigned". Examiner respectfully disagrees. The maximum limit imposed by the operating system for requested memory is a pre-assigned element because it is an element that has been established when a comparison with a requested memory occurs. Therefore, by the broadest reasonable interpretation, Frank's teaching of the maximum limit imposed by the operating system for requested memory can be construed to teach a pre-assigned maximum number of allocated blocks.

Applicant further argues that the memory allocation disclosed in Frank is not related to a hash table, and a person of skill in the art would have no reason or motivation to look to any teaches in Frank to cure the deficiencies of Hariguchi and Douceur (PRE-APPEAL BRIEF, page 4). Examiner respectfully disagrees. Hariguchi teaches the use of hash tables which requires an amount of memory for storing route entries (see column 6, line 66 – column 7, line 2; column 8, line 56 - column 9, lines 7;

and 160 in Fig. 4). Douceur teaches a hash table is allocated a group of memory blocks based on a size of the respective hash table (see column 19, line 23 – 26; line 62 - 67). Frank teaches allocating memory based on a maximum value supported by the operating system, and memory is allocated based on the result of the comparison (see column 5, line 26 – 34). One of ordinary skill in the art at the time of the invention would be motivated to combine the teachings of Frank to Hariguchi and Douceur to improve efficiency in memory usage by limiting the memory blocks each hash table can be assigned.

Applicant further argues that neither Frank nor Douceur teaches an allocation based on the two different elements recited in claim 1 (see PRE-APPEAL BRIEF, 2nd paragraph in page 4 for definitions of the two different elements), and the two references cannot just be combined to render this two-element require as obvious. Examiner respectfully disagrees. Douceur teaches a hash table is allocated a group of memory blocks based on a size of the respective hash table (see column 19, line 23 – 26; line 62 - 67). Frank teaches allocating memory based on a maximum value supported by the operating system, and memory is allocated based on the result of the comparison (see column 5, line 26 – 34). Both Douceur and Frank provide the benefit of efficient usage of limited memory resource. Therefore, one of ordinary skill in the art would be motivated to combine Hariguchi, Douceur, and Frank.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BO HUI A. ZHU whose telephone number is (571)270-1086. The examiner can normally be reached on Mon-Thu 10am-7pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Banks Marsha can be reached on (571)2727905. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/BO HUI A ZHU/
Examiner, Art Unit 2465